PSoC® Creator™
Project Datasheet for PWM_LED

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1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, PWMs, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 4200 family member PSoC 4 device. For details on all the systems listed above, please refer to the PSoC 4 Technical Reference Manual .

Figure 1. PSoC 4200 Device Family Block Diagram

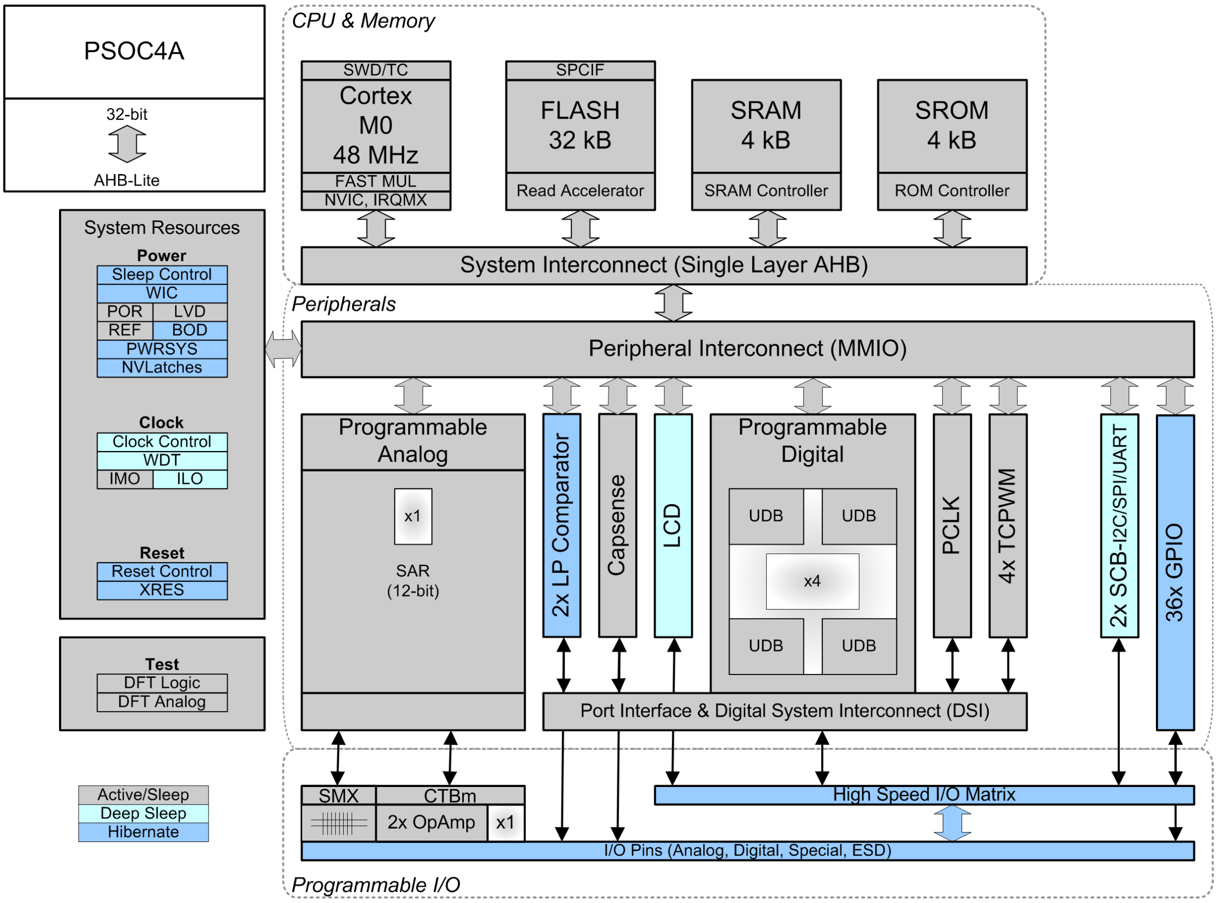


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Architecture	PSoC 4
Family	PSoC 4200
CPU speed (MHz)	48
Flash size (kBytes)	32
SRAM size (kBytes)	4
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

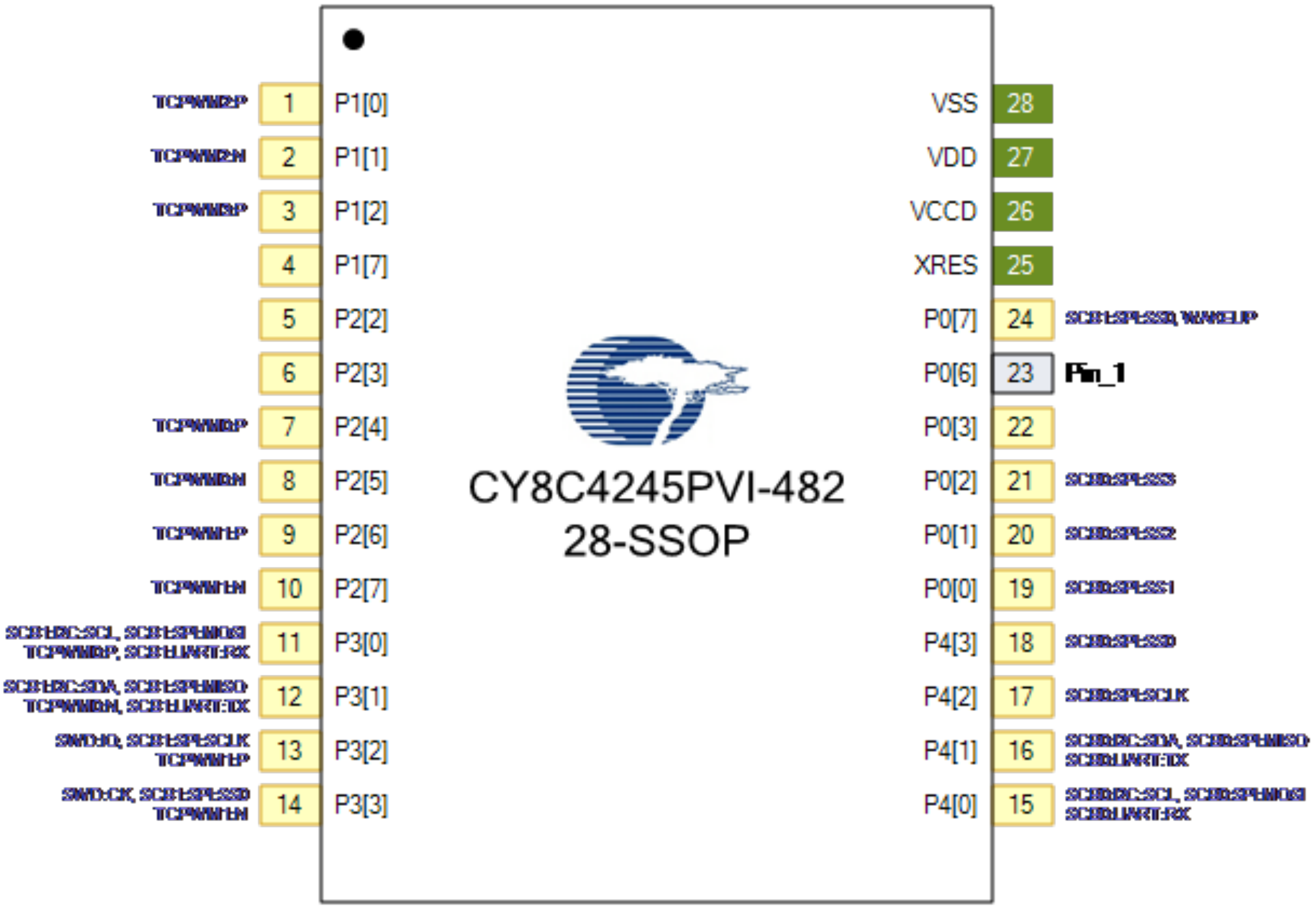
Table 2. Device Resources

Name	Resources in Use	Total Resources Available
Digital clock dividers	1 (25.0%)	4
Pins	1 (4.2%)	24
UDB Macrocells	11 (34.4%)	32
UDB Unique Pterms	10 (15.6%)	64
UDB Datapath Cells	2 (50.0%)	4
UDB Status Cells	2 (50.0%)	4
UDB Control Cells	2 (50.0%)	4
Interrupts	0 (0.0%)	32
Comparator/Opamp Fixed Blocks	0 (0.0%)	1
SAR Fixed Blocks	0 (0.0%)	1
CSD Fixed Blocks	0 (0.0%)	1
CapSense Blocks	0 (0.0%)	1
8-bit CapSense IDACs	0 (0.0%)	1
7-bit CapSense IDACs	0 (0.0%)	1
Temperature Sensor	0 (0.0%)	1
Low Power Comparator	0 (0.0%)	2
TCPWM Blocks	0 (0.0%)	4
Serial Communication Blocks	0 (0.0%)	2
Segment LCD Blocks	0 (0.0%)	1

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P1[0]	GPIO [unused]			HiZ Analog Unb
2	P1[1]	GPIO [unused]			HiZ Analog Unb
3	P1[2]	GPIO [unused]			HiZ Analog Unb
4	P1[7]	GPIO [unused]			HiZ Analog Unb
5	P2[2]	GPIO [unused]			HiZ Analog Unb
6	P2[3]	GPIO [unused]			HiZ Analog Unb
7	P2[4]	GPIO [unused]			HiZ Analog Unb
8	P2[5]	GPIO [unused]			HiZ Analog Unb
9	P2[6]	GPIO [unused]			HiZ Analog Unb
10	P2[7]	GPIO [unused]			HiZ Analog Unb
11	P3[0]	GPIO [unused]			HiZ Analog Unb
12	P3[1]	GPIO [unused]			HiZ Analog Unb
13	P3[2]	GPIO [unused]			HiZ Analog Unb
14	P3[3]	GPIO [unused]			HiZ Analog Unb
15	P4[0]	GPIO [unused]			HiZ Analog Unb
16	P4[1]	GPIO [unused]			HiZ Analog Unb
17	P4[2]	GPIO [unused]			HiZ Analog Unb
18	P4[3]	GPIO [unused]			HiZ Analog Unb
19	P0[0]	GPIO [unused]			HiZ Analog Unb
20	P0[1]	GPIO [unused]			HiZ Analog Unb
21	P0[2]	GPIO [unused]			HiZ Analog Unb
22	P0[3]	GPIO [unused]			HiZ Analog Unb
23	P0[6]	Pin_1	Dgtl Out	Strong drive	HiZ Analog Unb
24	P0[7]	GPIO [unused]			HiZ Analog Unb
25	XRES	XRES	Power		
26	VCCD	VCCD	Power		
27	VDD	Power			
28	VSS	VSS	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

Name	Port	Type	Reset State
Pin_1	P0[6]	Dgtl Out	HiZ Analog Unb
Power	VDD		

Abbreviations used in Table 4 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 5. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x0100
Stack Size (bytes)	0x0400
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 6. System Debug Settings

Name	Value
Chip Protection	Open
Debug Select	GPIO

3.3 System Operating Conditions

Table 7. System Operating Conditions

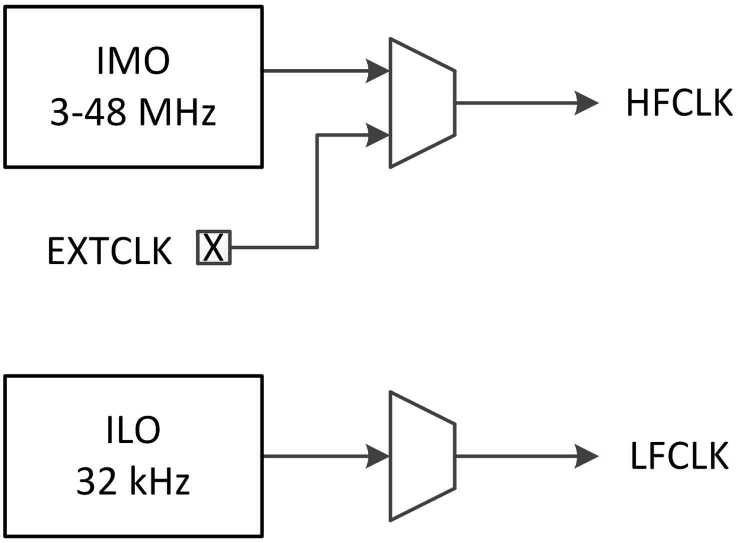
Name	Value
Vddd (V)	5
Vdda (V)	5
Variable Vdda	False
Temperature Range	-40C - 85C

4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±2% at 3 MHz
  - 32 kHz Internal Low Speed Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twelve clock dividers, each with 16-bit divide capability:
  - Eight can be used for fixed-function blocks
  - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
LFCLK	NONE	ILO	0	0.032	±30	True	True
ILO	NONE		0.032	0.032	±30	True	True
SYSCLK	NONE	HFCLK	0	24	±2	True	True
EXTCLK	NONE		24	0	±0	False	False
IMO	NONE		24	24	±2	True	True
HFCLK	NONE	Direct_Sel	24	24	±2	True	True

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

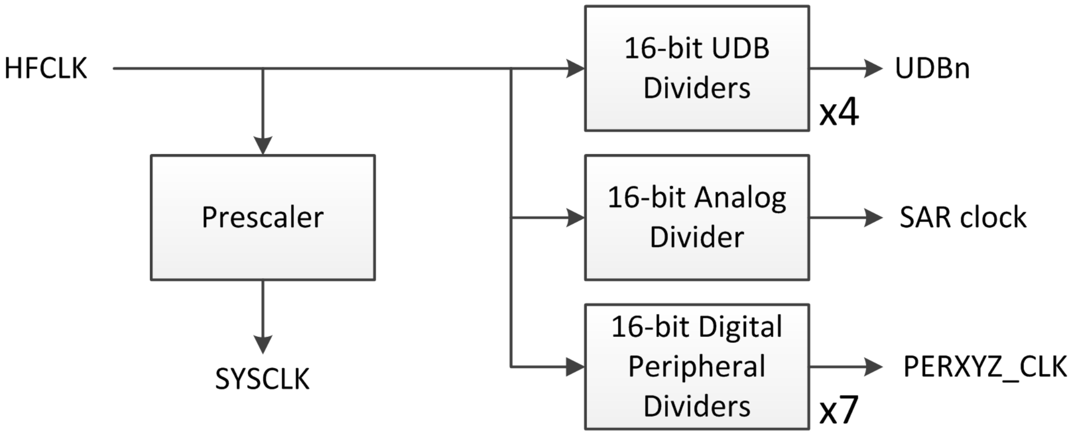


Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
Clock_1	DIGITAL	HFCLK	0.024	0.024	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyIMO API routines
  - CyILO API routines

5 Interrupts

5.1 Interrupts

This design contains no interrupt components.

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 10 lists the Flash protection settings for your design.

Table 10. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x7FFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 128 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

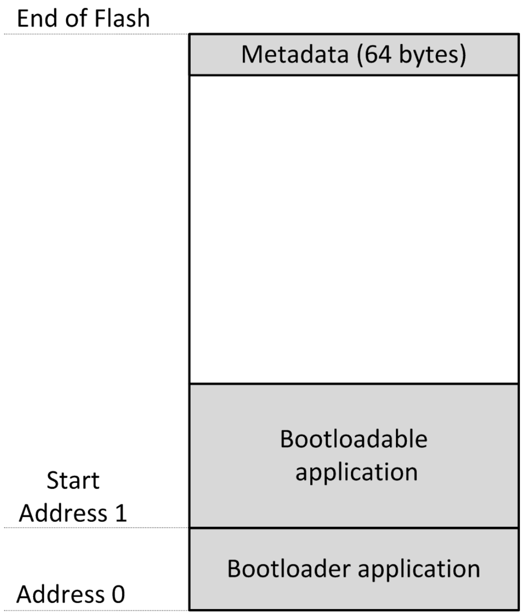
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 11. Bootloadable Settings

Name	Value
Application Version	0x0000
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x1080
Application Image 1 End Address	0x7F7F
Manual Application Image Placement	False

7.2 Bootloader Application

Table 12. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0000
Bootloader Start Address	0x0
Bootloader End Address	0x1030

For more information on the bootloader and startup please refer to:

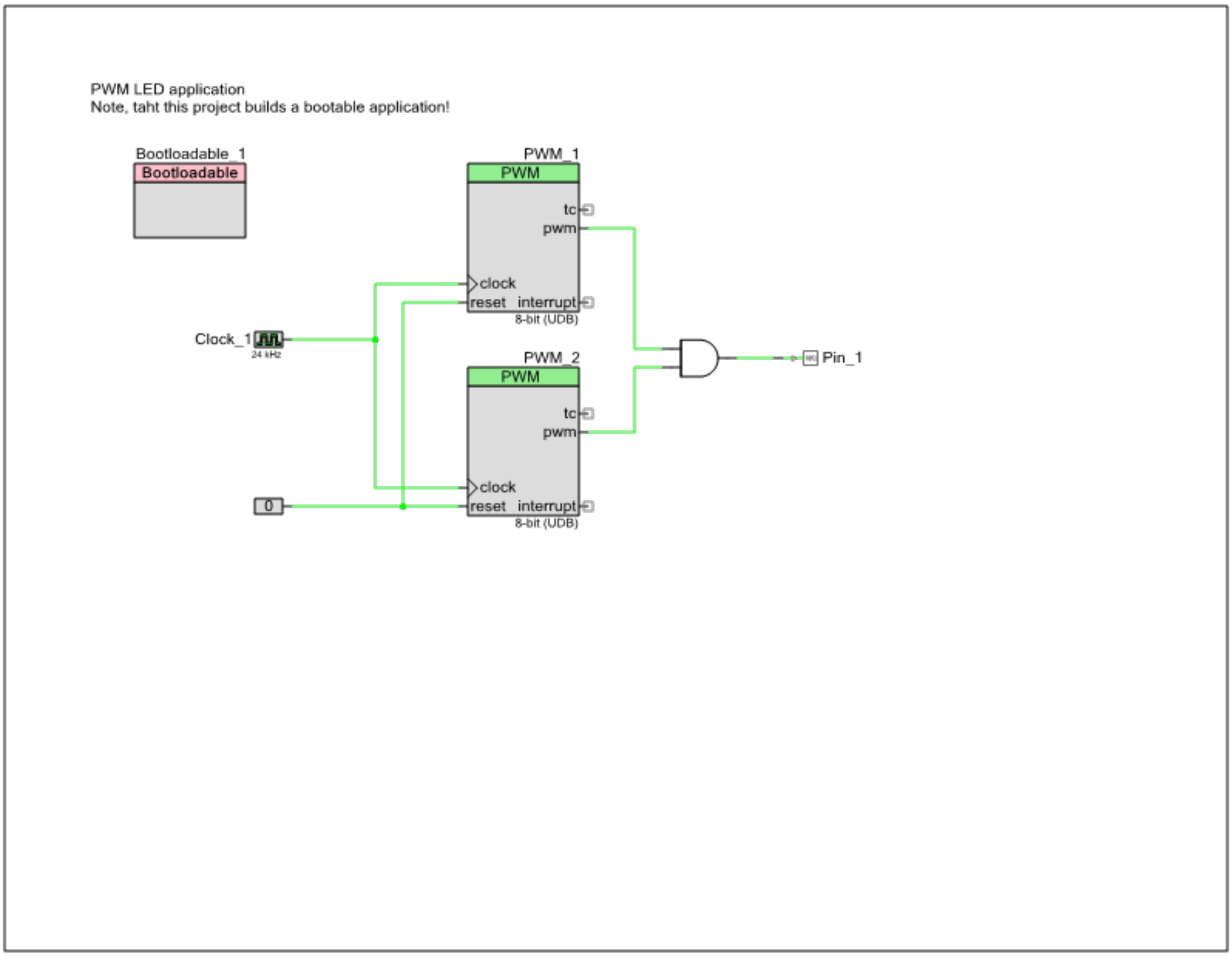
- Startup and Linking chapter in the System Reference Guide
- Datasheet for Bootloader and Bootloadable component

8 Design Contents

This design's schematic content consists of the following schematic sheet:

8.1 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance Bootloadable_1 (type: Bootloadable_v1_20)
- Instance PWM_1 (type: PWM_v3_0)
- Instance PWM_2 (type: PWM_v3_0)

9 Components

9.1 Component type: Bootloadable [v1.20]

9.1.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.
Instance type: Bootloadable [v1.20]
Datasheet: online component datasheet for Bootloadable

Table 13. Component Parameters for Bootloadable_1

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	0	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	0	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	true	Provides a method for PSoC Creator to place Bootloadable application image at a specified location. If true, image will be placed automatically. If false, image will be placed at address specified by Placement Address option.
elfFilePath	..\..\SCB_Bootloader\Dependencies\UART_Bootloader.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\..\SCB_Bootloader\Dependencies\UART_Bootloader.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows to specify address where the bootloadable application will be placed in memory. Available only if Automatic Application Image Placement option is true.

9.2 Component type: PWM [v3.0]

9.2.1 Instance PWM_1

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.0]
Datasheet: online component datasheet for PWM

Table 14. Component Parameters for PWM_1

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Greater or Equal	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	127	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	255	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	8	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

9.2.2 Instance PWM_2

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.0]
Datasheet: online component datasheet for PWM

Table 15. Component Parameters for PWM_2

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Greater or Equal	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	127	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	254	Defines the PWM period value

Parameter Name	Value	Description
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	8	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
    - Software base types
    - Hardware register types
    - Compiler defines
    - Cypress API return codes
    - Interrupt types and macros
- Registers
    - The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference Manual
    - Register Access chapter in the System Reference Guide
        - CY_GET API routines
        - CY_SET API routines
- System Functions chapter in the System Reference Guide
    - General API routines
    - CyDelay API routines
    - CyVd Voltage Detect API routines
- Power Management
    - Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
    - Low Power Modes chapter in the PSoC 4 Technical Reference Manual
    - Power Management chapter in the System Reference Guide
        - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
    - CyWdt API routines