PSoC® Creator™
Project Datasheet for LCD_scope

Creation Time: 09/16/2013 09:14:32
User: lenovo\cserny
Project: LCD_scope

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Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through Serial Wire Debug (SWD), and Single Wire Viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Family Block Diagram

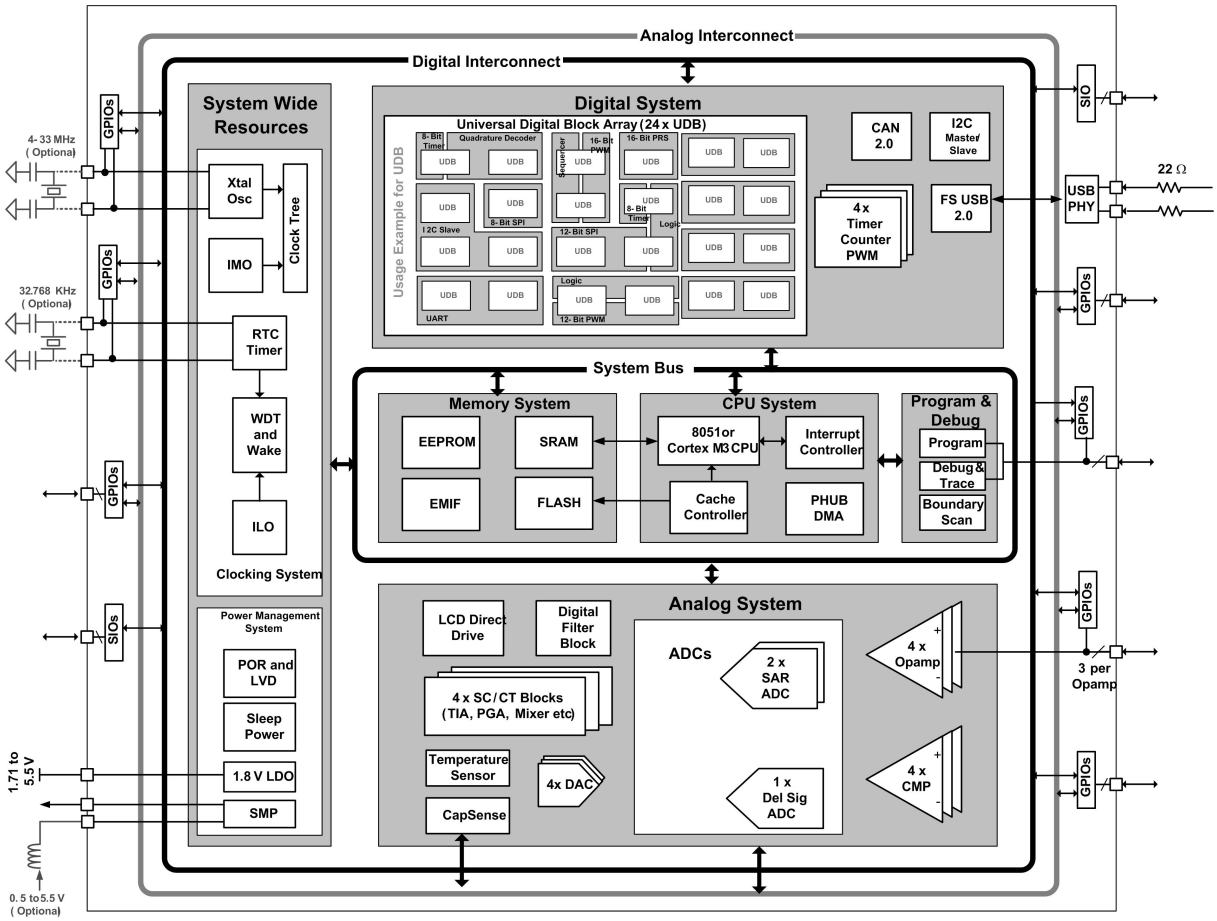


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Architecture	PSoC 5LP
Family	CY8C58LP
CPU speed (MHz)	67
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	0
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E123069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by BUS_CLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

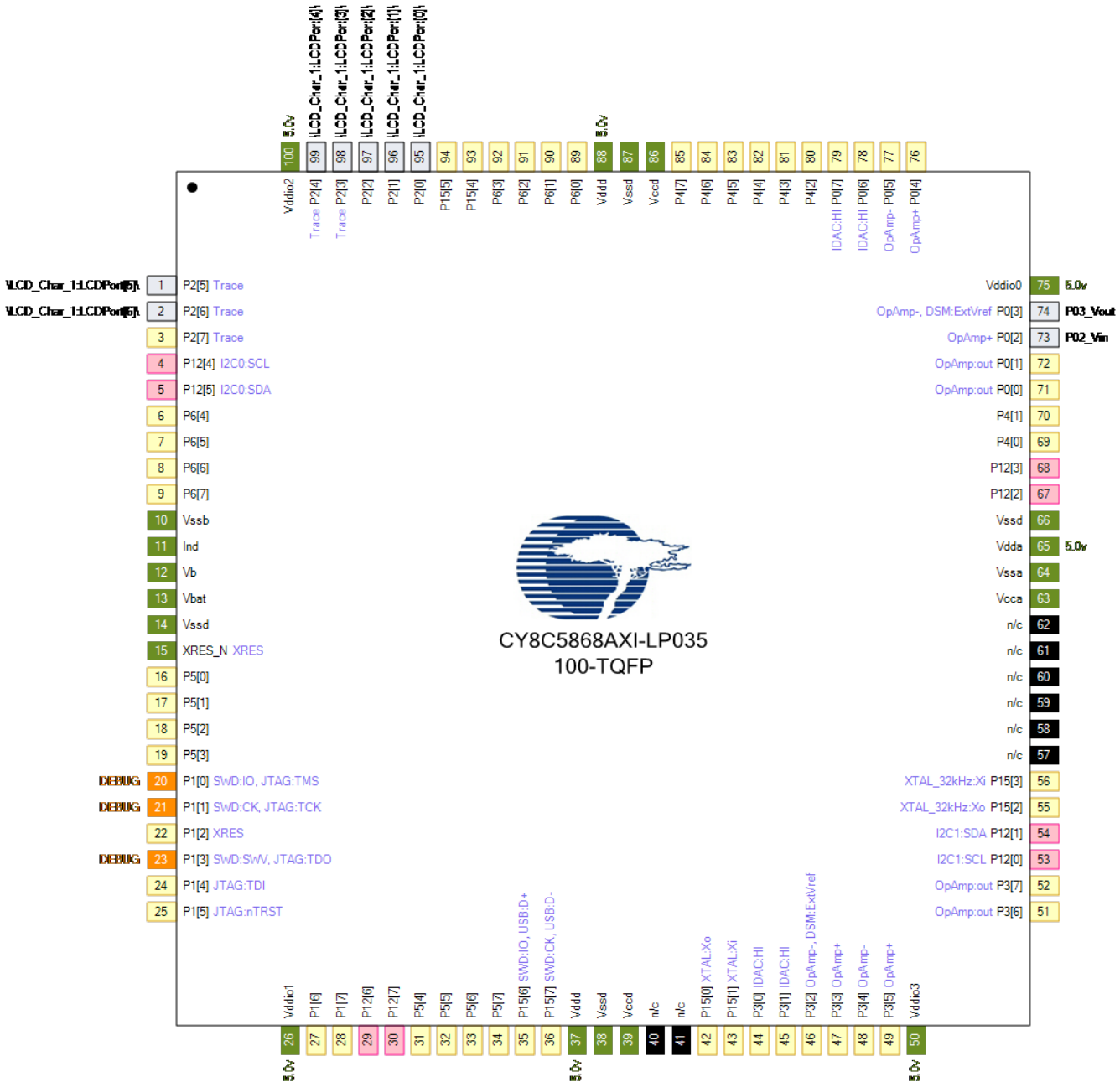
Table 2. Device Resources

Name	Resources in Use	Total Resources Available
Digital domain clock dividers	2 (25.0%)	8
Analog domain clock dividers	1 (25.0%)	4
Pins	12 (16.7%)	72
UDB Macrocells	1 (0.5%)	192
UDB Unique Pterms	0 (0.0%)	384
UDB Datapath Cells	0 (0.0%)	24
UDB Status Cells	0 (0.0%)	24
UDB Control Cells	0 (0.0%)	24
DMA Channels	0 (0.0%)	24
Interrupts	2 (6.3%)	32
DSM Fixed Blocks	1 (100.0%)	1
VIDAC Fixed Blocks	1 (25.0%)	4
SC Fixed Blocks	0 (0.0%)	4
Comparator Fixed Blocks	0 (0.0%)	4
Opamp Fixed Blocks	0 (0.0%)	4
CapSense Buffers	0 (0.0%)	2
CAN Fixed Blocks	0 (0.0%)	1
Decimator Fixed Blocks	1 (100.0%)	1
I2C Fixed Blocks	0 (0.0%)	1
Timer Fixed Blocks	0 (0.0%)	4
DFB Fixed Blocks	0 (0.0%)	1
USB Fixed Blocks	0 (0.0%)	1
LCD Fixed Blocks	0 (0.0%)	1
EMIF Fixed Blocks	0 (0.0%)	1
LPF Fixed Blocks	0 (0.0%)	2
SAR Fixed Blocks	0 (0.0%)	2

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	\LCD_Char_1:LCDPort[5]\		Strong drive	HiZ Analog Unb
2	P2[6]	\LCD_Char_1:LCDPort[6]\		Strong drive	HiZ Analog Unb
3	P2[7]	GPIO [unused]			HiZ Analog Unb
4	P12[4]	SIO [unused]			HiZ Analog Unb
5	P12[5]	SIO [unused]			HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	Vssb	Vssb	Power		
11	Ind	Power			
12	Vb	Vb	Power		
13	Vbat	Vbat	Power		
14	Vssd	Vssd	Power		
15	XRES_N	XRES_N	Power		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	GPIO [unused]			HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	GPIO [unused]			HiZ Analog Unb
21	P1[1]	GPIO [unused]			HiZ Analog Unb
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	Vio1	Vio1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	GPIO [unused]			HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	GPIO [unused]			HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB [unused]			HiZ Analog Unb
36	P15[7]	USB [unused]			HiZ Analog Unb
37	Vddd	Vddd	Power		
38	Vssd	Vssd	Power		
39	Vccd	Vccd	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	Vio3	Vio3	Power		
51	P3[6]	GPIO [unused]			HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	Vcca	Vcca	Power		
64	Vssa	Vssa	Power		
65	Vdda	Vdda	Power		
66	Vssd	Vssd	Power		
67	P12[2]	SIO [unused]			HiZ Analog Unb
68	P12[3]	SIO [unused]			HiZ Analog Unb
69	P4[0]	GPIO [unused]			HiZ Analog Unb
70	P4[1]	GPIO [unused]			HiZ Analog Unb
71	P0[0]	GPIO [unused]			HiZ Analog Unb
72	P0[1]	GPIO [unused]			HiZ Analog Unb
73	P0[2]	P02_Vin	Analog	HiZ analog	HiZ Analog Unb
74	P0[3]	P03_Vout	Analog	HiZ analog	HiZ Analog Unb
75	Vio0	Vio0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	GPIO [unused]			HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	GPIO [unused]			HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	Vccd	Vccd	Power		
87	Vssd	Vssd	Power		
88	Vddd	Vddd	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	GPIO [unused]			HiZ Analog Unb
94	P15[5]	GPIO [unused]			HiZ Analog Unb
95	P2[0]	\LCD_Char_1:LCDPort[0]\		Strong drive	HiZ Analog Unb
96	P2[1]	\LCD_Char_1:LCDPort[1]\		Strong drive	HiZ Analog Unb
97	P2[2]	\LCD_Char_1:LCDPort[2]\		Strong drive	HiZ Analog Unb
98	P2[3]	\LCD_Char_1:LCDPort[3]\		Strong drive	HiZ Analog Unb
99	P2[4]	\LCD_Char_1:LCDPort[4]\		Strong drive	HiZ Analog Unb
100	Vio2	Vio2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- HiZ analog = High impedance analog

2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

Name	Port	Type	Reset State
\LCD_Char_1:LCDPort[0]\	P2[0]		HiZ Analog Unb
\LCD_Char_1:LCDPort[1]\	P2[1]		HiZ Analog Unb
\LCD_Char_1:LCDPort[2]\	P2[2]		HiZ Analog Unb
\LCD_Char_1:LCDPort[3]\	P2[3]		HiZ Analog Unb
\LCD_Char_1:LCDPort[4]\	P2[4]		HiZ Analog Unb
\LCD_Char_1:LCDPort[5]\	P2[5]		HiZ Analog Unb
\LCD_Char_1:LCDPort[6]\	P2[6]		HiZ Analog Unb
P02_Vin	P0[2]	Analog	HiZ Analog Unb
P03_Vout	P0[3]	Analog	HiZ Analog Unb
Power	Ind		

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 5. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x1000
Stack Size (bytes)	0x4000
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 6. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Require XRES Pin	True
Use Optional XRES	False

3.3 System Operating Conditions

Table 7. System Operating Conditions

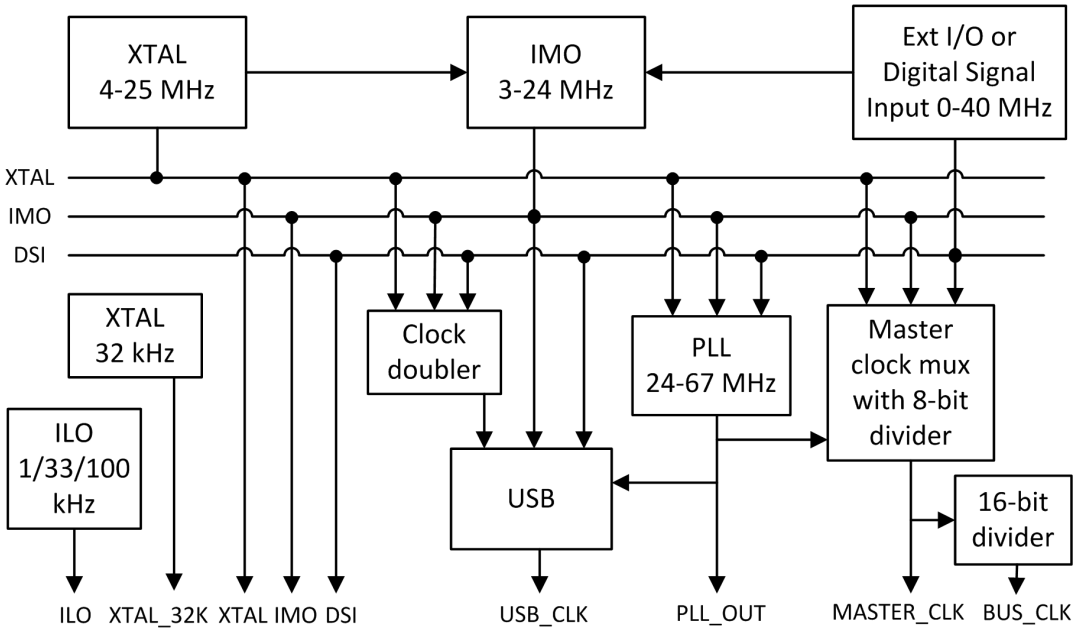
Name	Value
Vddd (V)	5.0
Vdda (V)	5.0
Variable Vdda	False
Vddio0 (V)	5.0
Vddio1 (V)	5.0
Vddio2 (V)	5.0
Vddio3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±5% at 3 MHz
  - 1 kHz, 33 kHz, 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - USB Clock Domain, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
USB_CLK	DIGITAL	IMO	48	0	±0	False	False
BUS_CLK	DIGITAL	MASTER_CLK	0	24	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	0	24	±1	True	True
Digital Signal	DIGITAL		0	0	±0	False	False
XTAL 32kHz	DIGITAL		0.0328	0	±0	False	False
XTAL	DIGITAL		25	0	±0	False	False
ILO	DIGITAL		0	0.001	-50,+100	True	True
PLL_OUT	DIGITAL	IMO	24	24	±1	True	True
IMO	DIGITAL		3	3	±1	True	True

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

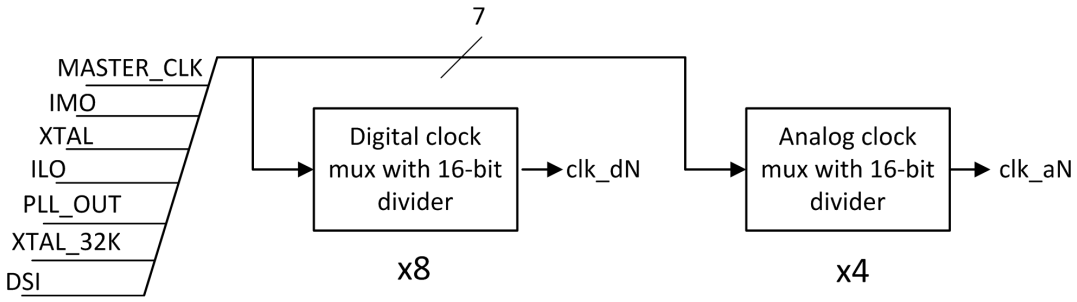


Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
clock_1	DIGITAL	IMO	0.0003	0.0003	±1	True	True
ADC_DelSig_-1_theACLK	ANALOG	MASTER_CLK	0.156	0.1558	±1	True	True
ADC_DelSig_-1_Ext_CP_Clk	DIGITAL	MASTER_CLK	1	1	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines

- CyMaster API routines
- CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 10. Interrupts

Name	Priority	Vector
ADC_DelSig_1_IRQ	7	29
isr_1	7	0

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 11 lists the Flash protection settings for your design.

Table 11. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

For more information on Flash memory and protection, please refer to:

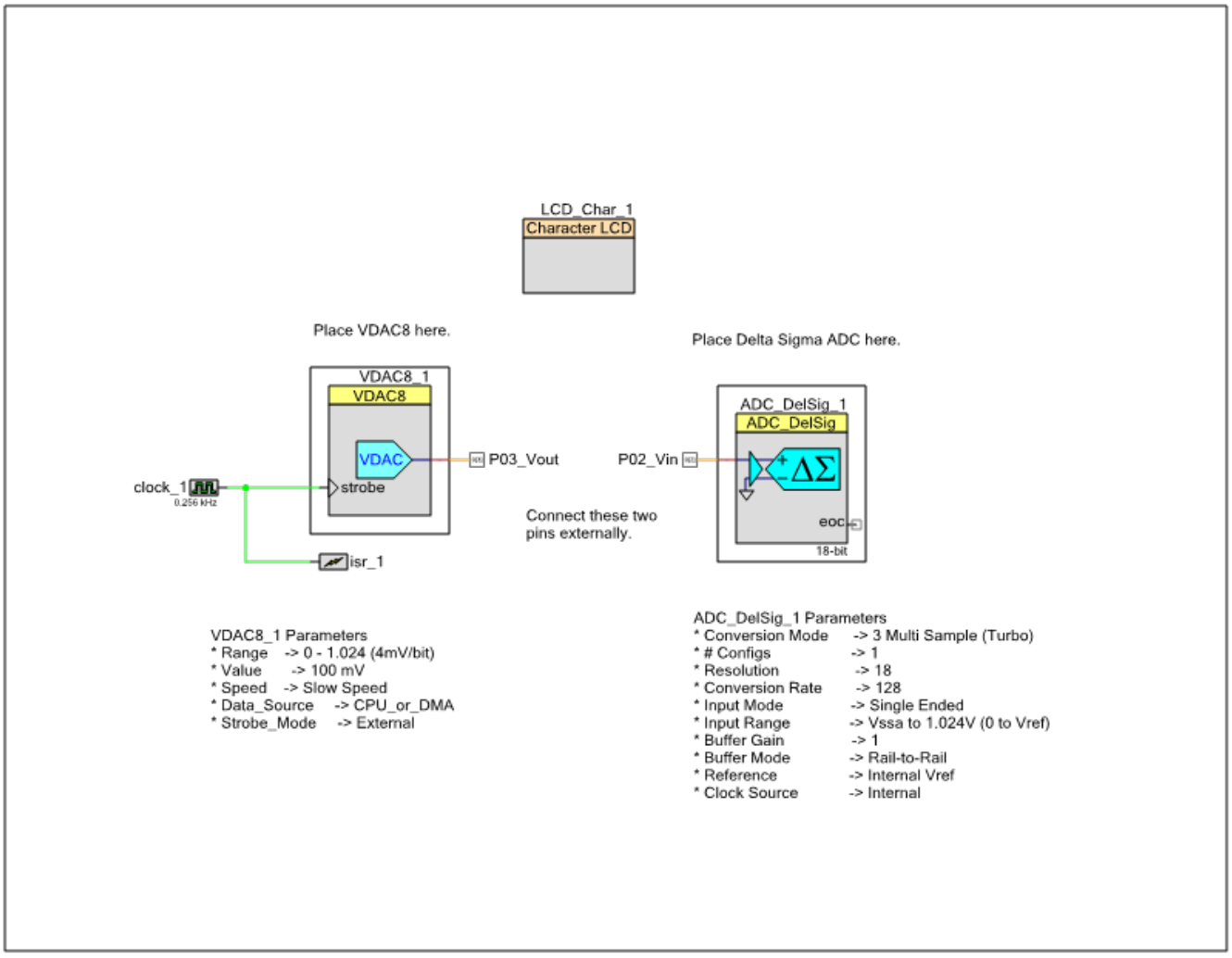
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance ADC_DelSig_1 (type: ADC_DelSig_v2_30)
- Instance LCD_Char_1 (type: CharLCD_v1_90)
- Instance VDAC8_1 (type: VDAC8_v1_90)

8 Components

8.1 Component type: ADC_DelSig [v2.30]

8.1.1 Instance ADC_DelSig_1

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v2.30]
Datasheet: online component datasheet for ADC_DelSig

Table 12. Component Parameters for ADC_DelSig_1

Parameter Name	Value	Description
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	Vssa to 1.024V (0.0 to Vref)	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	18	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.

Parameter Name	Value	Description
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	3 - Multi Sample (Turbo)	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.024	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
Sample_Rate	128	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
sRate_Err	false	Parameter to hold the Conversion rate error status of ADC configuration.
Start_of_Conversion	Software	Continuous conversions or hardware controlled

8.2 Component type: CharLCD [v1.90]

8.2.1 Instance LCD_Char_1

Description: Character LCD Component
Instance type: CharLCD [v1.90]
Datasheet: online component datasheet for CharLCD

Table 13. Component Parameters for LCD_Char_1

Parameter Name	Value	Description
ConversionRoutines	true	Defines if the conversion routines will be included in the project.
CUSTOM0	0,E,8,8,8,E,0	Defines encoded representation of first custom character of the user-defined font.
CUSTOM1	0,A,A,4,4,4,0	Defines encoded representation of second custom character of the user-defined font.
CUSTOM2	0,E,A,E,8,8,0	Defines encoded representation of third custom character of the user-defined font.
CUSTOM3	0,E,A,C,A,A,0	Defines encoded representation of fourth custom character of the user-defined font.
CUSTOM4	0,E,8,C,8,E,0	Defines encoded representation of fifth custom character of the user-defined font.
CUSTOM5	0,E,8,E,2,E,0	Defines encoded representation of sixth custom character of the user-defined font.
CUSTOM6	0,E,8,E,2,E,0	Defines encoded representation of seventh custom character of the user-defined font.
CUSTOM7	0,4,4,4,0,4,0	Defines encoded representation of eighth custom character of the user-defined font.
CustomCharacterSet	Vertical bargraph	Defines the type of custom character set (User defined, Vertical or Horizontal bargraph). Based on the selection a look-up table with proper characters representation will be generated in the source code.

8.3 Component type: VDAC8 [v1.90]

8.3.1 Instance VDAC8_1

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 14. Component Parameters for VDAC8_1

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.
Initial_Value	25	Configures the initial vDAC output voltage. The output uses the following relation: Initial output voltage = value*(FullRange/255). This calculated output voltage value is invalid if DAC Bus is used.

Parameter Name	Value	Description
Strobe_Mode	External	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 1.020V (4mV/bit)	Specifies the full voltage scale range of the vDAC
VDAC_Speed	Low Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	100	This parameter sets the voltage value.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine